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The Development and Reliability of Small Pitch Flip Chip on Flex Process

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Abstract

In portable electronics product business there is a strong trend towards miniaturization. At the same time when the size and the weight of these products are decreasing the number of functions and the performance is increasing. This trend towards miniaturization means that the packaging density is increasing significantly. Target of our research was to develop small pitch flip chip on flex process for electronic module applications.

This paper presents the results from the reliability tests of different types of flexible substrates and different types of anisotropically conductive adhesives in high-density flip chip application. The reliability of the samples was tested using thermal shock tests and 85/85 test. Cross section samples were made to analyze the possible failure mechanism of failed contacts. Two different test devices were used (bump sizes 50x50µm and 50x90µm). The effective pitch was 80 µm in both samples and the number of contacts was around 200. The contact resistance was measured with four-point method and the series resistance with daisy chain method. The results are a part of European Union supported development project.

Introduction

Flexible printed circuit boards are used more and more in high density applications like in smart cards, hearing aids, LCD modules and other modules used in portable electronics. Common to all of these applications is small pitch and use of flip chip technology. The main reasons for the interest towards flexible printed circuit boards and flip chip technology in addition to high density/small pitch capability is the need to reduce weight and space, eliminate connectors and get more flexibility in design.

In ACA flip chip the electrical contact between the pad and the bump is mechanical unlike in solder flip chip. In typical bonding process ACA material is taped (film type) or dispensed (paste type) to the bonding area of the substrate and the chip is aligned and pressed against the bonding pads. The adhesive is cured in elevated temperature and the pressure is maintained during the whole curing time. To decrease the total cycle time in some case the bonding is done in few steps. In such case the IC is aligned and pre bonded to the substrate and the final curing is done on the second phase.

Materials in Flip Chip on Flex

Anisotropically conductive adhesives are composite materials containing typically epoxy-based matrix and small amount of conductive particles. The adhesive itself doesn't conduct before processing unlike isotropically conductive adhesives, because the volume fraction of the conductive particles is relatively low and the particles are not in contact with each other. The adhesive begins to conduct in z-direction after the IC is pressed against the pads on the substrate. After the bonding process part of the particles are stuck and squeezed between the pad and the bump. These squeezed particles form an electrical conductive bridge between the IC and substrate. Conductive particles are typically metal flakes or spheres made of silver of nickel (hard particle) or metal coated plastic balls (soft particle). Soft and elastic metal (Ni/Au) coated polymer particle provides reliable electrical contact between the bump and the pad since it deforms under pressure and provides large contact area [1]. Hard metal particle doesn't normally deform so much but it can penetrate though the oxide layer on the conductor and form good contact.

The flexible printed circuit boards used in flip chip applications have either two-layer structure or three-layer structure. Two-layer structure or adhesiveless flexible PCB consists of thin and flexible dielectric substrate and copper foil. Three main technologies are usually applied for two layers continuous films production. In the first one a thin copper layer is evaporated or sputtered onto the dielectric surface (Kapton® or Upilex®) and an additional thick copper layer is electroplated. In the second one a liquid resin (epoxy or polyimide) is coated onto the copper layer and cured. In the third one an epoxy glass prepreg is laminated onto the copper layer and cured. Three-layer structure flexible PCB consists of thin and flexible dielectric substrate and copper foil which is laminated to the substrate with thin adhesive layer.

Especially in small pitch applications the most widely used substrate material is polyimide. The benefits of the polyimide (PI) are that it can tolerate relatively high temperatures, its dimensional stability is relatively good and the chemical resistance is high. Unfortunately the water absorption and the cost are relatively high. Other base materials that are used are polyester, polyethylene naphthalate (PEN) and epoxy-glass (EG). Polyester has excellent flexibility, good electrical properties, chemical resistance and low cost but the temperature stability is poor. The thermal stability of the polyethylene naphthalate is slightly better than polyester has but also the cost is higher. The benefit of epoxy-glass is low CTE and relatively low cost but the flexibility is poor compared to other flex materials. One new and interesting base material is liquid crystalline polymer (LCP).

Important factors when selecting dielectric substrates are mechanical strength, flexibility, dimensional stability, dielectric properties, thermal properties, chemical resistance, moisture absorption and cost [2,3].

Reliability and electrical performance of ACA interconnection

The reliability and electrical performance of the flip chip on flex interconnection is a result from the several factors. The key factors are the process parameters (bonding temperature, bonding time, bonding pressure), the adhesive (matrix, particles) and the substrate material. To achieve reliable contact the adhesive must be cured properly. Otherwise the long time reliability of the connections is not good enough and mechanical and chemical properties, for example humidity resistance of the adhesives, are not sufficient. Also the mechanical and chemical properties of the adhesive and the compatibility of the materials has strong effect to the reliability. The adhesion to the IC and flex and mechanical strength of the adhesive must be good so that the structure can tolerate stress caused for example by the thermal mismatch of the materials. Moisture can cause reliability problems to the flip chip interconnection, like oxidation and swelling, and due to that the moisture resistance of the polymer matrix should be very good. The ideal conductive particle has good mechanical reliability, very good conductivity and high resistance toward oxidation and corrosion. Particles that are mainly used can be divided in to two categories that are soft particles and hard ones. Particle should be hard enough that it will break the possible oxide layer and make good mechanical contact with the bump and the pad. Nevertheless, soft and flexible particle can compensate the possible small height variations and co-planarity problems [4-7].

Both the contact area and the surface of the IC must be clean to avoid reliability and adhesion problems. The number of the particles in the contact and the degree of the deformation of the particles should be high enough to achieve low contact resistance [8].

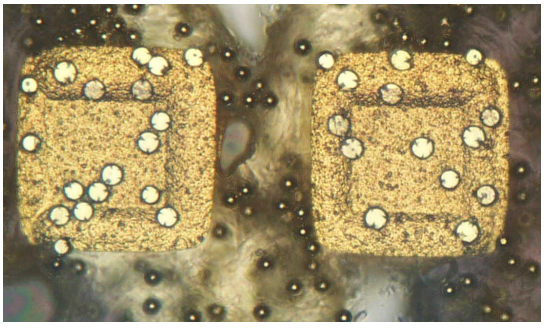

Figure 1. The interconnection between a glass substrate and the test chip (80 µm pitch).

The Figure 1 shows an example of a good and reliable electrical contact, which requires that enough high number of conductive particles are trapped between the bump and the pad. This can be achieved by using large contact areas or high conductive particle density. In small pitch applications the contact area can not be large and thus the particle density must be higher so that a low contact resistance can be achieved (Figure 2).

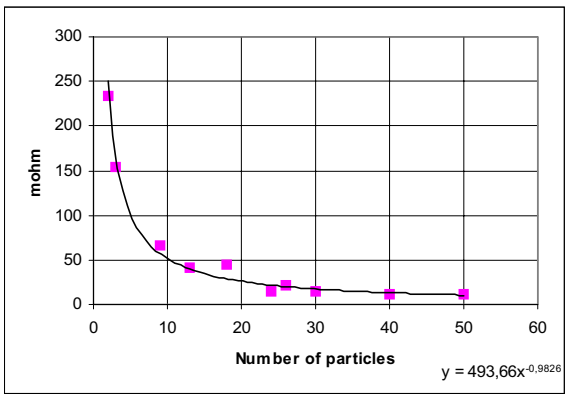

Figure 2. The contact resistance of the ACF joint as a function of the number of conductive particles in the interconnection.

However high particle density increases the risk of short cuts. The risk of short cuts has been minimized by using insulation layer around the conductive particles or by orientating the particles with magnetic field. The bonding pressure must be optimized according to the number and size of the bumps and the size of the IC to achieve low contact resistance. Too high pressure will squeeze the soft particles too much and break the metal coating while too low pressure can cause high contact resistance due too low degree or deformation of the particle. The pressure should be high enough to avoid also the problems caused by the height variations of the conductors and bumps [1].

Test materials and test procedure

The adhesive used in these tests was selected according to previous tests. The matrix of the adhesive was a mixture of different epoxy resins and the conductive particles were Ni/Au plated polymer particles with insulation layer.

Two different base materials were used in the test flexes: UPILEX-75S and EPOXY GLASS G10 halogen free. The thickness of the PI was 75 µm and of EG 110 µm. A picture of the test flex is shown in Figure 3.

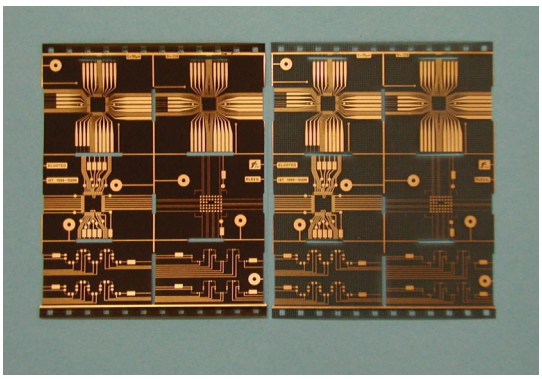

Figure 3. The picture of test flex used in the tests.

The copper was 18 µm thick ED copper film that was laminated to the PI test flex with 12 µm thick adhesive and to the EG flex with 18 µm thick adhesive. Both flexes were coated with 0,5 µm nickel and 0,075 µm gold layers. The plating of the flex was done using electroplating process. Test flexes were manufactured by FCI Microelectronics. The heat shrinkage of EG was slightly larger than of PI.

Both test IC's were Au bumped and the number of the I/Os was approximately 200. The bumps in test IC1 were in one row and in test IC2 in two rows (contact area 50x50µm and 50x90µm). The effective pitch was 80 µm in both IC's. Both IC's contains measurement structures to measure contact resistance (four-point probe) and daisy chain resistance. The height of the Au bumps was 20 µm and the bumping was done in Elcoteq Network Corporation.

Flip chip components were bonded to the test flexes using accurate Toray FC-1000 flip chip bonder. Bonding parameters were according to the ACF manufacturer's recommendation.

The reliability of the interconnection was tested using standard 85%RH/85°C test and –40- +125 °C thermal shock test. The total number of the shocks was 1000. Shock test was done in two-chamber cabin and the extreme temperatures were –40 °C and +125 °C. Samples were in both extreme temperatures 14 minutes and the transfer time was 1 minute. Samples were measured in both extreme temperatures every 30 seconds and during the transfer every 10 seconds. During the 85%RH/85°C test the samples were measured every 10 hours. The total length of the test was 1000 hours.

Results and discussion

The Daisy chain resistance measurements during the 85%RH /85°C test are shown in the Figure 4. As can be seen from the results no increases in the contact resistance values were noticed during 1000 hours.

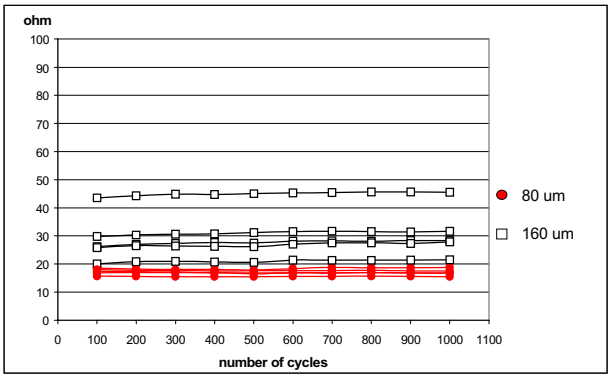

Figure 4. 85 /85 test results of EG and PI test flexes.

No evident differences were noticed between the different base materials and bump pitches. No remarkable change in contact resistance could be seen after 1000 hours.

The results from the shock test of polyimide test substrates are shown in Figure 5. No major increase in contact resistances were occurred during 1000 cycles with PI flexes and no differences in the reliability between 80 µm bump pitch and 160 µm bump pitch were noticed.

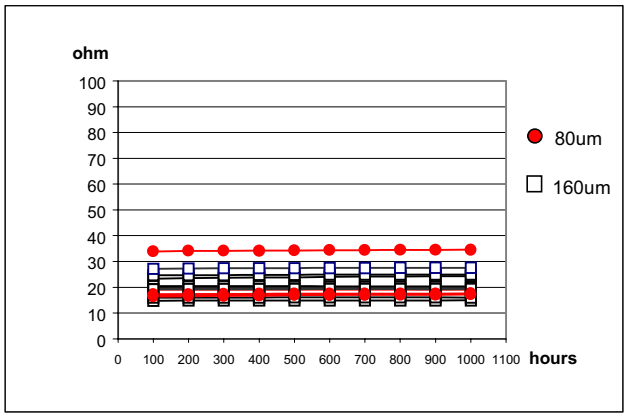

Figure 5. Thermal shock test results of PI test flex.

The results from the shock test of epoxy glass substrate are shown on the Figure 6. As can be seen from the figure below the 80 µm bump pitch didn't pass the test. The contact resistance started to increase clearly already after 100 cycles. The performance of 160 µm bump pitch samples was considerably better. The contact resistance values were relatively stable even the value in part of the samples increased slightly.

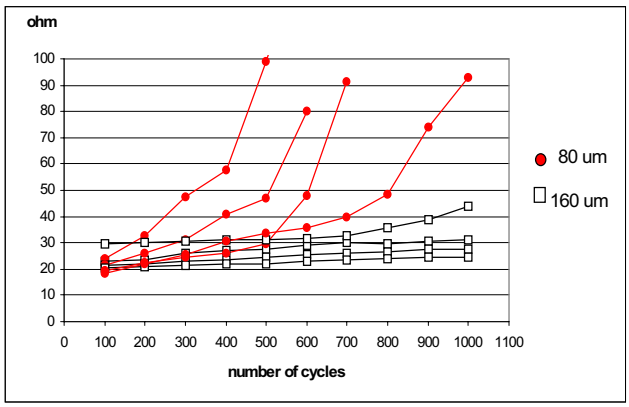

Figure 6. Thermal shock test results of EG test flex.

In the Figure 7 the measured correlation of the contact resistance of the Daisy chain resistance is shown.

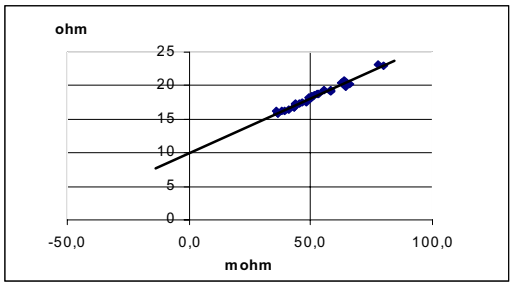

Figure 7. Relationship between the Daisy chain resistance (ohm) and the contact resistance (mohm).

Using the relationship presented in Figure 7 the changes in contact resistance can easily be calculated when the Daisy chain resistance is known.

According to the results the base material and the layout of the bumps and the pads seems to have effect to the reliability. Larger contact area gives higher reliability, at least in certain case, most likely due to higher amount of the compressed particles between the pad and the bump.

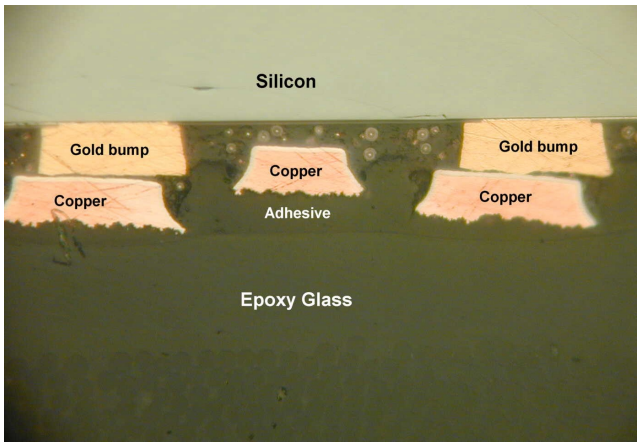

Figure 8. Interconnection using EG.

As can be seen from Figure 8, the copper conductor sinks into the adhesive that is between the conductors and EG substrate due to high pressure and elevated temperature used during bonding cycle. Figure 9 shows that the sinking effect is very small in case of polyimide substrate. According to the cross section pictures the adhesive and the unhomogeneous structure of the base material, like in case of epoxy glass (glass fiber core), has effects to the tendency of the conductor sinking.

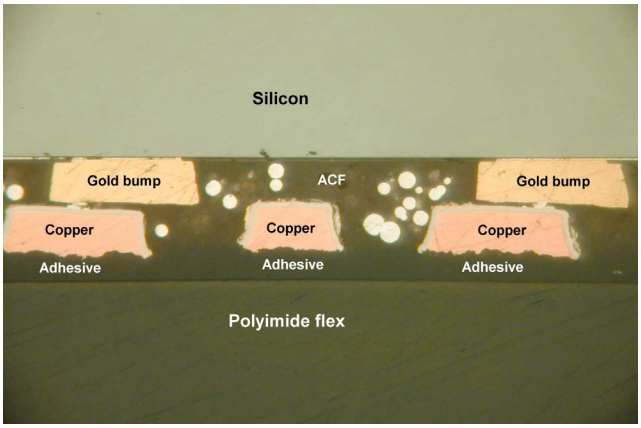

Figure 9.Interconnection using PI.

This phenomenon explains partly the differences in the reliability test results between EG- and PI- substrates. This phenomenon is not as critical in case of 160 µm bump pitch test IC where the pad is larger and also due to that the contact area is bigger. To minimize the sinking of the contact pad, the pad should be as large as possible.

With suitable adhesive, which can withstand the bonding temperature and pressure without softening and giving in too much is one alternative.

Conclusions

According to the tests the reliability of flip chip on polyimide flex is higher than flip chip on epoxy glass flex. All flip chip on polyimide flex samples passed the reliability tests without any failures or major increase in the contact resistance. No differences in reliability were noticed between 80 µm and 160 µm samples. In 85%RH/85°C test no failures or differences in reliability between 80 µm and 160 µm flip chip on epoxy glass flex were noticed. In thermal cycling test the samples of 80 µm flip chip on epoxy glass flex failed. The contact resistance started to increase clearly already after 100 cycles. However no major increase in contact resistance were noticed with 160 µm samples.

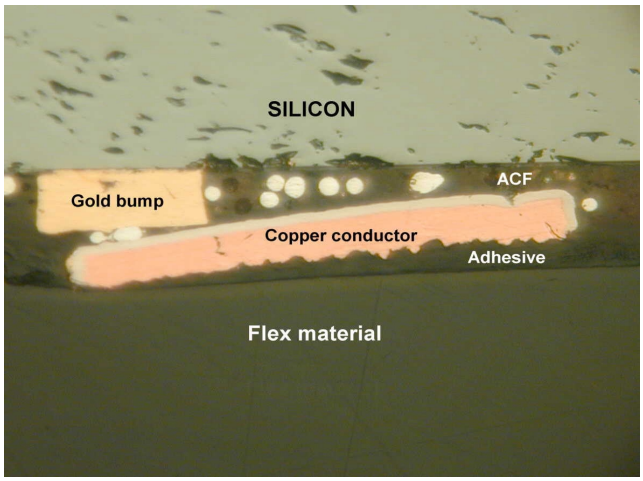

Figure 10. The sinking of the copper conductor during the bonding process.

In the several cross sectional samples made of the failed devices no cracks or delamination could be seen. However the strong sinking of the contact pads could be seen in the epoxy glass flexes (Figure 10). So this could be an explanation for the failures in the temperature cycling tests.

According to the results the base material and the layout of the bumps and the pads seems to have effect to the reliability. Larger contact area gives higher reliability, at least in certain case, most likely due to higher amount of the compressed particles between the pad and the bump.

With suitable substrate materials and layout the sinking of the conductors into the substrate is smaller and due to that the reliability is higher.

Acknowledgement

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Mechanical Fatigue Tests of Solder Joint under Mixed-mode Loading Cases

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Abstract

To give a proper and accurate estimation of the fatigue life of solder joints, a mechanical fatigue test under mixed-mode loading cases is proposed. The loading phase is controlled by the angle of loading direction. Experiments are conducted with eutectic 63SnPb solder joints. The isothermal mechanical fatigue tests were performed under conditions of several loading phases. Constant displacement controlled tests are performed using a micro-mechanical test apparatus. Failure patterns of the fatigue tests are observed and discussed.

Introduction

The use of surface mount components has been increased, because modern electronics technology requires complex, high density, high speed devices. Due to this high degree of integration, high component density, and the resulting high production cost of the surface mount technology, the modern advanced SMC assembly has imposed more stringent reliability requirements on packaging design.

Service failure of solder interconnections generally arises due to thermomechanical fatigue (TMF) and usually occurs within the solder itself since this is the softest component of the joint. The combination of temperature fluctuations, either due to power switching or the external environment, and materials in the joint which possess different coefficients of thermal expansion, produce substantial cyclic strains within the solder. As a result of the mismatch coefficient of thermal expansion(CTE), the devices undergo not only shear deformation but also warpage and distortion during thermal excursions encountered in manufacturing process and actual operting conditions[1]. Moreover in some cases, such as mobile phones, the devices can be subjected to various mechanical and environmental stresses. Therefore in most applications, solder joints are not under pure shear or pure tensile loading. A relationship between shear and tensile deformation in needed to account for multiaxial stress states.

The changes in the mechanical test of solder joint have been reported by several researchers[2-4]. However, the mechanical test under mixed-mode loading cases has not been reported. Such a study would be helpful in understanding the solder joint reliability behavior.

In the present work, low cycle fatigue test of solder joints under mixed-mode loading cases was performed. Isothermal low cycle fatigue testing was performed with the machine that provides cyclic mixed-mode strain in the solder balls with varying loading phases. The loading phases are controlled by the angle of loading directions. The failure of the solder bump was detected with the load drop method and the resistance measurement. To apply various micromechanical load, a precise testing apparatus was developed. The test results were obtained at a fixed test temperature (25°C) but at different loading phases and different total strain level. As a fatigue model, the Morrow energy model was examined.

Micromechanical testing system

A general-purpose micro-mechanical test apparatus was developed for an experimental study on the reliability of electronic packaging. The automated testing system developed is schematically shown in Fig. 1, which consists of testing machine part, and a control and sensing part. The testing machine applies a load to the specimen via a servomotor attached to a ball screw driven rail table. The displacement of the specimen can be feedback controlled with the resolution of 50nm by a personal computer and data acquisition system. Fig 2 shows the calibration result of the displacement measured by LVDT attached in the grip using linear encoder. This calibration was performed under free-loading state. The stepwise signal shown in Fig. 2 is due to linear encoder resolution.

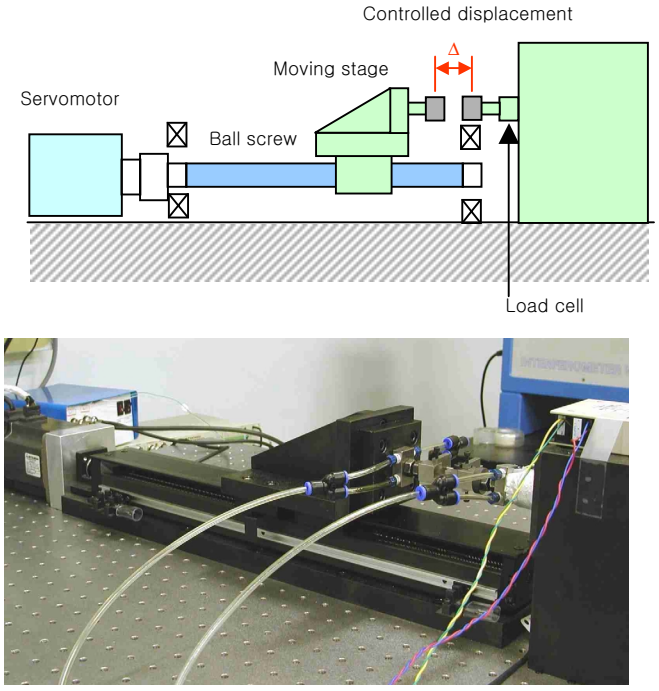


Fig. 1. Micromechanical testing system

The traveling range is up to 100 mm that depends on gripping system and testing style. The capacity of load cell is 50kgf and it's signal can be acquired with the resolution of ±2mV in the range of 10V. Using this system, it was possible to detect the failure of the interconnection very accurately by the load drop method and the resistance measurement.

Experimental procedure

Many reports on the mechanical properties of solder show that for a similar composition of solder alloy there are large variations in the solder mechanical properties due to the variation in the specimen's configurations and testing conditions[4]. Thus, in order to have a better understanding of the solder joint properties, it is important to study a displacmenent controlled mechanical test for a solder joint specimen similar in geometry, size and microstructure to the actual PBGA solder joints soldered on to the PWB. In this work, the fatigue specimen consists of a ball grid array component, reflow solder attached to a mating printed circuit board(PCB). Sn/Pb eutectic solder balls (diameter 0.76mm) with 1.27mm pitch were mounted to soldermask defined FR-4 PCBs. The PCB pads were diameter of 0.787mm (31mil), solder mask opening diameter of 0.584mm (24mil), and of copper of 35∓m thickness, plated with 5∓m of nickel, and a less than 1∓m gold flash (Fig. 3). The specimen was formed using the reflow process in a reflow oven. The reflow temperature profile is shown in Fig 4.

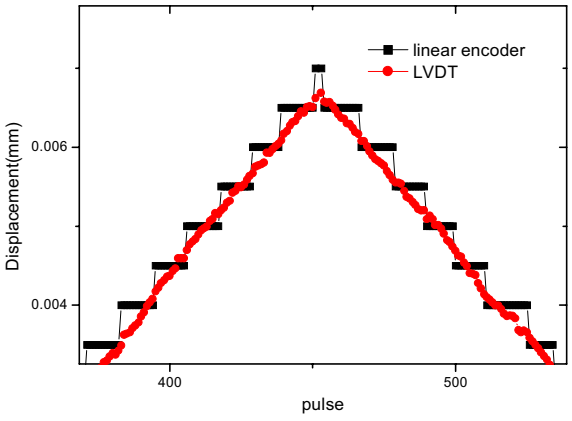
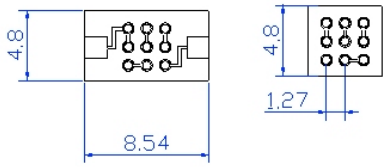
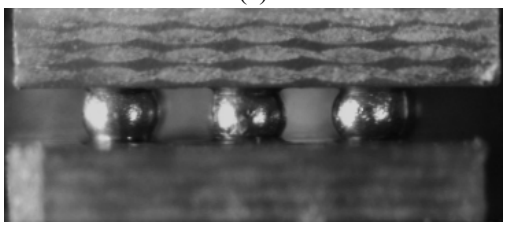


Fig. 2. Calibration with linear encoder



(a)



(b)

Fig. 3. (a) Specimen dimensions (mm) and (b) reflowed solder shape

The 9 solder balls in a specimen are connected within a series circuit that is monitored for continuity. The resistance change resulting from the applied cyclic strain in the testing is measured during the cyclic fatigue testing. The resistance is measured using Wheatstone resistance bridge. Fig. 5 shows the Wheatstone bridge circuit consisting of four resistor arms including the specimen daisy chain with a voltage source, an amplifier and a data acquisition system. Using the data acquisition system, the resistance signal was monitored and recorded at the desired time interval. For these fatigue tests, signals were recorded at the interval of 0.1 seconds, i.e., 200 points per cycle.

The fabricated specimens were bonded to steel grips using a cyanoacrylate adhesive. To change the loading phase, several grips are prepared as shown in Fig. 6. To increase machine stiffness and reduce out of plane forces, no other moving stage was used. Instead of the stage, a rigid alignment grip was used to align grips. An AC LVDT was used to measure the relative displacement between grips as shown in Fig. 7. The relative displacement was controlled with the resolution 50nm by a personal computer and data acquisition system. Various displacement control shape was possible. In present work, tests were performed at 0.05Hz sinusoidal displacement loading with changing the amplitude from 4∓m to 25∓m. The typical displacement and load profiles for a controlled displacement range test of 15 ∓m is shown in Figs. 8 and 9 respectively.

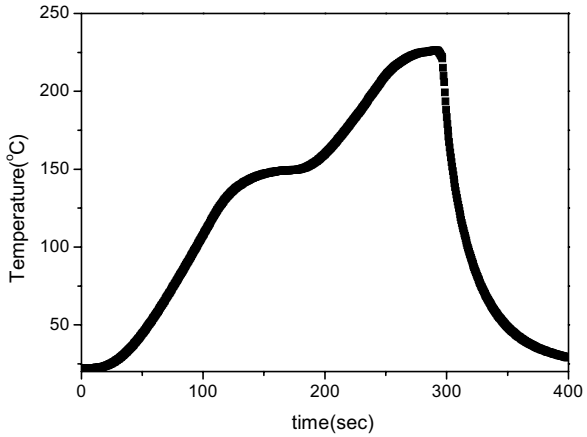


Fig. 4. Reflow temperature profile

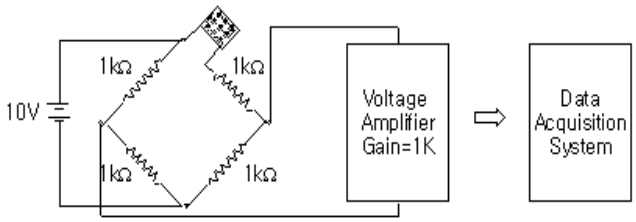


Fig. 5. Schematic circuit diagram to measure the change of the electrical resistance of the solder bumps

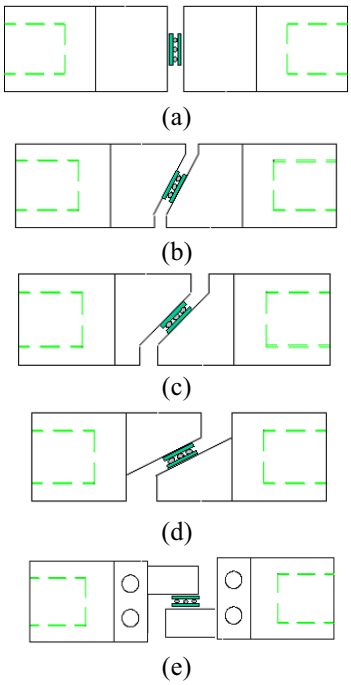


Fig. 6. Test grip configurations. Loading phase of each specimen is (a) 0^o (pure tension) (b) 27^o (c) 45^o (d) 63^o (e) 90^o(pure shear).

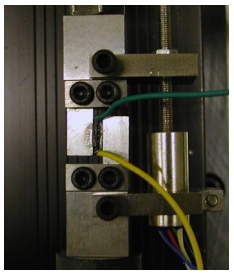


Fig. 7. AC LVDT and grips for measuring the relative displacement between specimen grips.

Experimental Results

The mechanical fatigue test under mixed-loading was performed in a displacement-controlled mode in which the specimen was subjected to a fully reversed sinusoidal mixed load at a constant frequency of 0.05 Hz. The applied displacement on the specimen was controlled to be constant until failure occurred. Several specimens on each loading case were tested at various displacement amplitudes.

To determine the lifetime of the specimens, the change in resistance was recorded at a rate of 10 scans per second. A typical resistance vs. cycles curve is compared with load drop in Fig. 10. As the cycles increased, the magnitude of the resistance became larger. The increase in the resistance is caused by fatigue damage accumulation in the solder bumps. As shown in Fig. 10, there are abrupt increases in the resistance at 50% load drop. However this phenomina was not consistent throughout the whole experiments. This abrupt increase in the resistance occurred from 50% to 80% load drop depending on the loading phase. Therefore in present work, fatigue life was defined by 50% load drop.

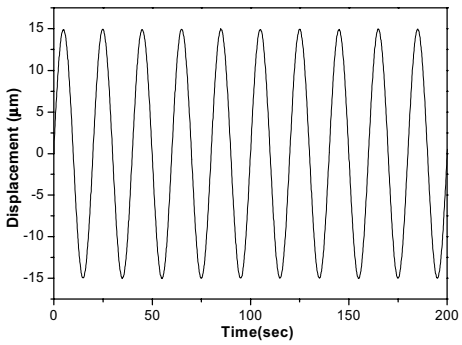


Fig. 8. Displacement vs. time profile

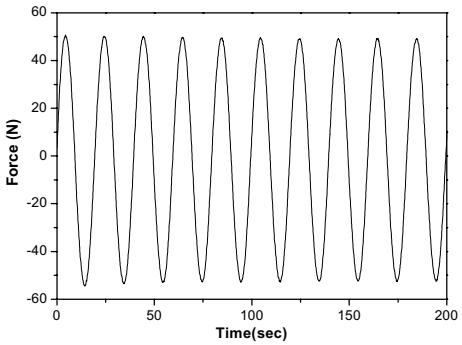


Fig. 9. Force vs. time profile

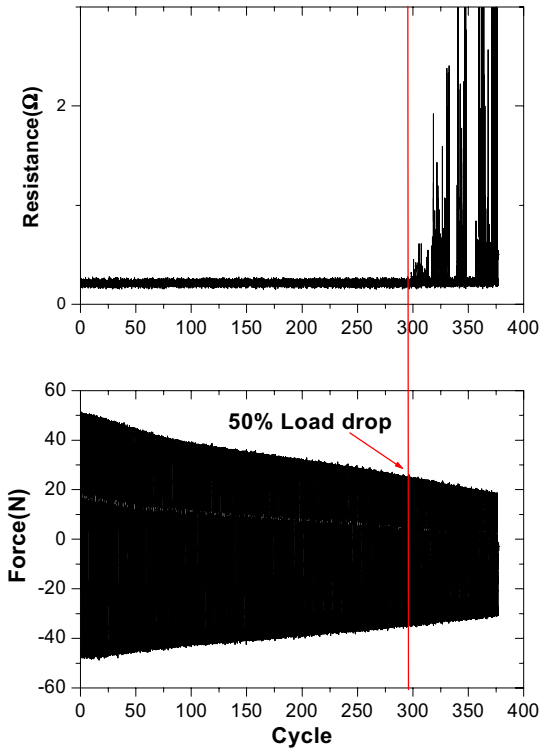


Fig. 10. A typical resistance vs. cycles curve and correspoding load drop curve as cycle increases.

Throughout the whole test every load versus displacement hysteresis was recorded with a rate of 200 scans per cycle. The material behaviour under 4±μm constant displacement control is shown in Fig. 11. Force displacement response is very different between the different loading phases. In the 0^o loading phase, i.e., pure tension compression loading case, the force displacement ratio is very stiff.

The force amplitude decreased with the number of cycles in the course of the test as shown in Fig. 12. Typical hysteresis curves of the first and subsequent cycle are shown in Figs. 13,14 and 15. The area inside the hysteresis refers to the plastic work dissipated by the solder material. This work effects either microstructural changes or crack propagation. Throughout the all load phase, the first cycle hysteresis is symmetric in compression and tension loading area. However in the case of a later subsequent cycle, some asymmetric hysteresis are shown except pure shear test. This asymmetric refer to the touch of two corresponding fracture surfaces in the cracked area. Both surfaces are pressed against each other when in compress loading. Excluding this distortion in compression loading, the hysteresis is almost symmetric in compression and tension loading.

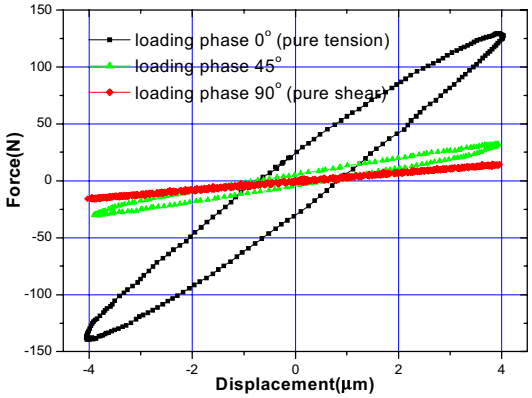


Fig. 11. Force vs. displacement at 4 ∓m displacement stroke.

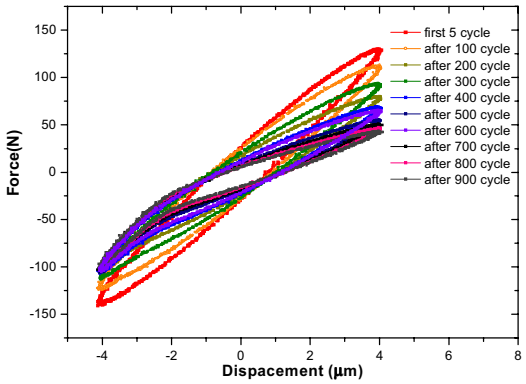


Fig. 12. Applied loading decreases as cycle increases. (in 0^o loading phase)

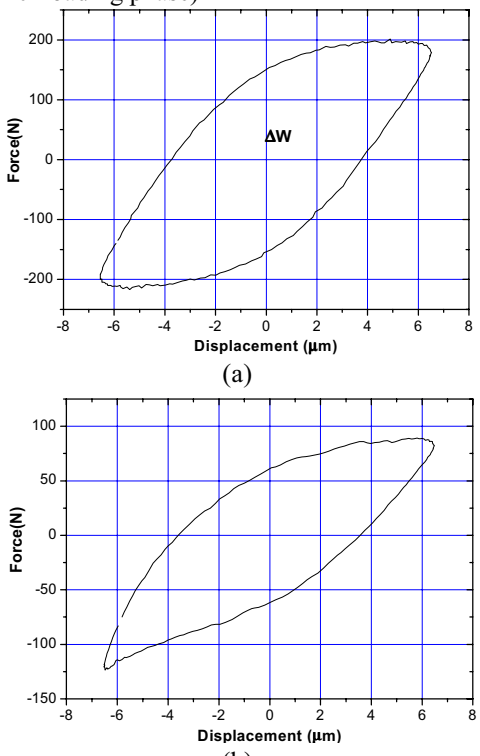
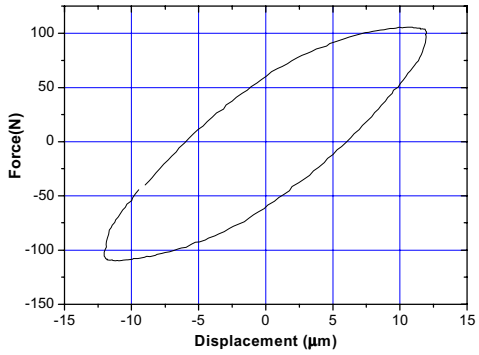
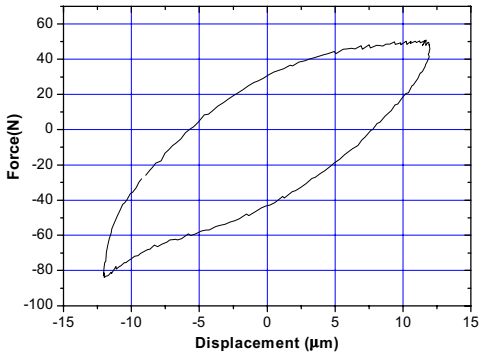


Fig. 13. Force-displacement hysteresis at (a) 1st cycle (b) 50% load drop in 0^o loading phase

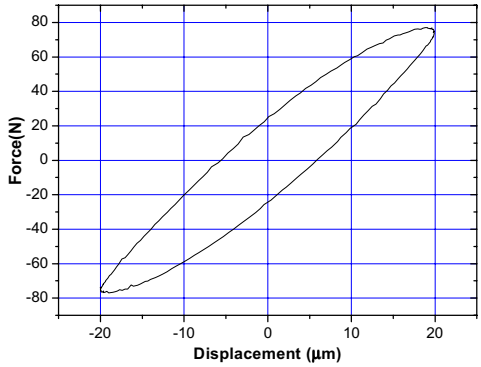


(a)

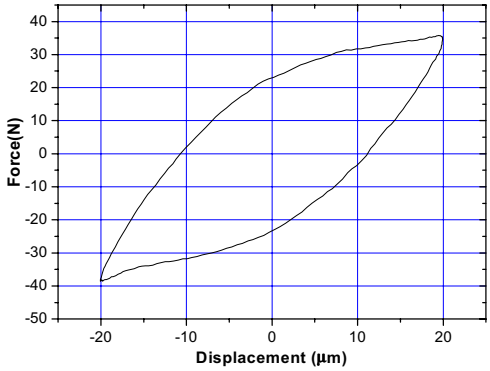


(b)

Fig. 14. Force-displacement hysteresis at (a) 1st cycle (b) 50% load drop in 45° loading phase



(a)



(b)

Fig. 15. Force-displacement hysteresis at (a) 1st cycle (b) 50% load drop in 90° loading phase

The correlation of life cycles versus displacement stroke is shown in Fig. 16. The fatigue life curve of solder bumps with various displacement stroke becomes straight lines within same loading phase. Between the loading phases, however, there are apparent discrepancy.

As a fatigue model, the Morrow energy mode was examined[6-7]. The model predict fatigue life(N_f) in terms of the plastic strain energy density ΔW, as shown below:

$$N_f^m \Delta W = C \tag{1}$$

where m is fatigue exponent, and C is material ductility coefficient. The plastic strain energy density was determined from the area within the first stabilized hysteresis loop. Fig. 17 shows fatigue life of the eutectic alloy as a function of strain energy density. The results in Fig. 17 were obtained at a fixed test temperature (25°C) but at different loading phases and different total strain level. The Morrow model predicts a linear relationship between $\log N_f$ and $\log \Delta W$ irrespective to loading phase.

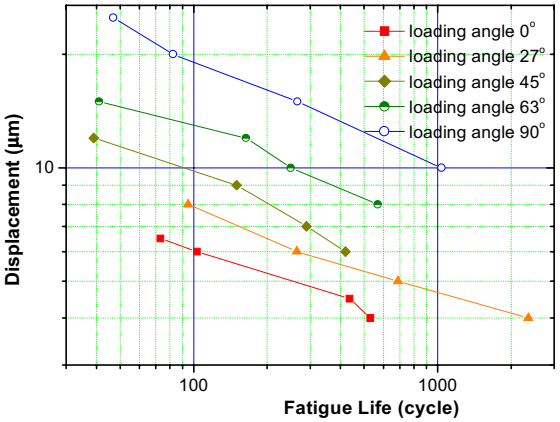


Fig. 16. Fatigue life versus Displacement stroke

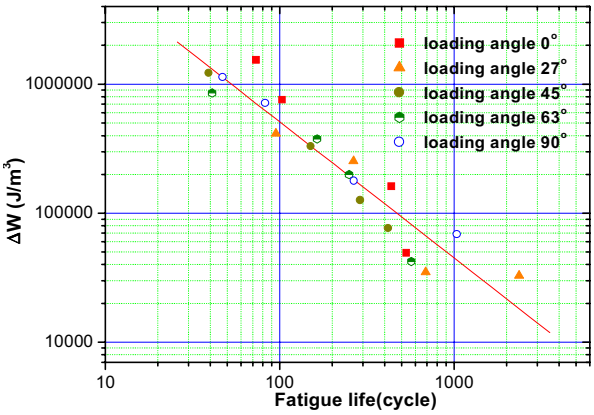


Fig. 17. Fatigue life versus strain energy density

Conclusions

To apply various micromechanical load, a precise testing apparatus was developed. Isothermal low cycle fatigue testing was performed with the machine that provides cyclic mixed-mode strain in the solder balls with varying loading phases. The loading phases are controlled by the angle of loading directions. Low cycle fatigue test of solder joints at room temperature under mixed-mode loading cases was performed. The failure of the solder bump was detected with the load drop method and the resistance measurement. Throughout the whole test every load versus displacement hysteresis was recorded with a rate of 200 scans per cycle. Force displacement response is very different between the different loading phases.

As a fatigue model, the Morrow energy model was examined. The model predicts a linear relationship between $\log N_f$ and $\log \Delta W$ irrespective to loading phase.

Acknowledgments

This work has been supported by Computer Aided Reliability Evaluation(CARE) for Electronic Packaging - National Research Laboratory (NRL) program.

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Shear Strength and Aging Characteristics of Sn-Pb and Sn-Ag-Bi Solder Bumps

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Abstract

Ball shear strength and aging charcteristics of the 63Sn-37Pb solder bumps were characterized with variations of UBM finish (Au/Ni/Cu and Ni/Cu) and solder ball size (0.35 to 0.76 mm). Also, tensile strength, ball shear strength, and aging characteristics of the Sn-3.5Ag-Bi solder alloys were investigated. When formed on Au/Ni/Cu UBM, ball shear strength of the 63Sn-37Pb solder bumps of 0.35 mm size was higher than those of the 0.62 and 0.76 mm sizes due to precipication hardening of Au-Sn intermetallic compounds. When the bump size was identical, the 63Sn-37Pb solder bumps exhibited higher shear strength on Au/Ni/Cu UBM than on Ni/Cu UBM. Shear strength of the 63Sn-37Pb solder bumps formed on Ni/Cu UBM was little varied with aging at 150°C up to 1000 hours. With increasing the aging time, the failure mode of the 63Sn-37Pb solder bumps on Au/Ni/Cu UBM was changed from ductile fracture (solder failure) to brittle fracture (interface failure). The 63Sn-37Pb solder bumps on Ni/Cu UBM showed ductile fracture regardless of the aging time up to 1000 hours. Tensile strength of the Sn-3.5Ag-Bi alloys increased with increasing the Bi content up to 9 wt%. Ball shear strength of the Sn-3.5Ag-Bi solder bumps increased with increasing the Bi content and reached maximum at 5-7 wt% Bi. Shear strength of the Sn-3.5Ag-5Bi solder bumps increased substatially from 70 MPa to 84 MPa by aging at 150°C for 300 hours.

Introduction

Solders play an indispensable role in joining materials and components in electronic devices [1,2]. As the size and pitch of the solder bumps decrease rapidly, the reliability of the package is more and more dependent on the solder joint reliability [3,4]. In general, ball shear test has been adapted to evaluate the solder bump reliability and to optimize the reflow process. Consequently, shear strength of the solder joint is considered as one of the critical factors that determine the solder bump reliability. Shear strength and aging characteristics of solder bumps are dependent upon the bump size, solder composition, and UBM structure [5-7].

In this study, shear strength and aging characteristics of the 63Sn-37Pb solder bumps were characterized with variations of UBM finish (Au/Ni/Cu and Ni/Cu) and solder ball size (0.35 to 0.76 mm). Also, tensile strength of the Sn-3.5Ag-Bi alloys was evaluated, and ball shear strength as well as aging characteristics of the Sn-3.5Ag-Bi solder bumps were investigated with addition of Bi up to 9 wt% to Sn-3.5Ag.

Experimental

Solder bumps of 63Sn-37Pb were formed by reflowing commercial solder balls of 0.35-0.76 mm size on UBM finishs of Au (0.5 μm)/Ni (5 μm)/Cu (27 μm) and Ni/Cu. The solder ball size, photo solder resiste (PSR) open size, and UBM surface finish combinations for solder bumps are listed in Table 1. The 63Sn-37Pb solder balls were reflowed at 220°C in a RMA flux ambient. During reflow, dwell time at the peak temperature(220°C) was changed from 30 seconds to 3,000 seconds.

Table 1. Experiment conditions for solder bumping.

Solder	Solder ball (mm)	PSR open (mm)	UBM
63Sn-37Pb	0.35	0.30	Au/Ni/Cu
	0.62	0.50	Au/Ni/Cu
	0.76	0.64	Au/Ni/Cu
	0.62	0.50	Ni/Cu
Sn-3.5Ag-Bi	0.76	0.64	Au/Ni/Cu

Sn-3.5Ag-Bi alloys were prepared with addition of 1-9 wt% Bi to the Sn-3.5Ag. Elemental metals were weighed for proper compositions, melted in the sealed quartz tubes under vacuum, and homogenized using rocking furnace at 800°C. The ingots were then re-melted at 240°C and cooled at the same rate of the reflow profile. The ingots were then machined to tensile specimens (Fig. 1) and tensile tests were carried out at a strain rate of 3×10^{-4}/s. To fabricate the solder bumps of 0.76 mm diameter, the Sn-3.5Ag-Bi alloys rolled to 0.2 mm thickness and then manually punched out to make coupons of 0.6 mm diameter. The reflow of the Sn-Ag-Bi solder bumps was carried out in a RMA flux ambient at 240°C for 30-180 seconds.

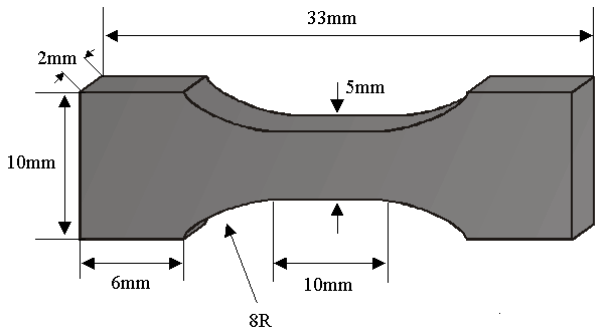

Fig. 1. Schematic illustration of tensile specimen.

Solder bumps of 63Sn-37Pb and Sn-Ag-Bi, which were reflowed for 60 seconds at the peak temperatures, were aged at 150°C up to 1000 hours. Ball shear tests for the 63Sn-37Pb and Sn-Ag-Bi solder bumps were conducted Dage-2400 shear tester. The ball height was kept at 0.05 mm above the solder mask surface, and the shear speed was 0.2 mm/s. For each experiemtal condition, more than 30 solder bumps were sheared off with accordance with the JEDEC standard [8]. The intermetallic layer thickness, microstructure and fracture surface of the 63Sn-37Pb and Sn-Ag-Bi solder bumps have been observed using SEM with backscattered electron image (BEI).

Shear strength and aging characteristics of the 63Sn-37Pb solder bumps

Fig. 2 shows the shear strength of the 63Sn-37Pb solder bumps as a function of the dwell time at 220°C. For the 63Sn-37Pb solder bumps formed on Au/Ni/Cu UBM, the shear strength increased with increasing the dwell time from 30 seconds to 60 seconds, and was little changed with further increase of the dwell time up to 3000 seconds.

As shown in Fig. 2, shear strength of the solder bumps of 0.35 mm size was higher than those of the 0.62 and 0.76 mm size. It has been known that Au is dissolved into 63Sn-37Pb solder rapidly because of the high solubility of Au atoms in the molten solder. At the typical reflow peak temperature, 63Sn-37Pb solder can dissolve more than 11 wt% Au [9]. Assuming that all Au in Au/Ni/Cu UBM intact to the solder bump was dissolved into the solder, Au concentration in each solder bump after the reflow was calculated and summarized in Table 2.

As shown in Table 2, Au concentration decreased with increasing the solder bump size. Thus, high shear strength of the solder bumps of 0.35 mm size could be attributed to precipication hardening with Au-Sn intermetallic compounds formed during cooling after reflow. Au-Sn intermetallic compounds in the solder matrix impede the dislocation movement, resulting in increasing the shear strength. As shown in Fig. 2, the shear strength of the solder bumps of 0.62 mm size, formed on Au/Ni/Cu UBM, is higher than those fabricated on Ni/Cu UBM, which implied precipitation hardening with Au-Sn compounds.

Table 2. Au concentration of 63Sn-37Pb solder bumps formed on Au/Ni/Cu UBM.

Solder Ball (mm)	Solder Ball Pad (mm)	Au Concentration (wt%)
0.35	0.30	4.40×10^{-3}
0.62	0.50	2.18×10^{-3}
0.76	0.64	1.93×10^{-3}

Fig. 3 shows the shear strength of the 63Sn-37Pb solder bumps, reflowed at 220 °C for 60 seconds, as a function of the aging time. Shear strength of the 63Sn-37Pb solder bumps, fabricated on Au/Ni/Cu UBM, decreased initially with increasing the aging time up to about 200 hours and then little decreased with further increase of the aging time. Although the initial shear strength of the 63Sn-37Pb solder bumps on Ni/Cu UBM was lower than that on Au/Ni/Cu, the shear strength of the solder bumps on Ni/Cu was almost same as the initial value even after aging for 1000 hours.

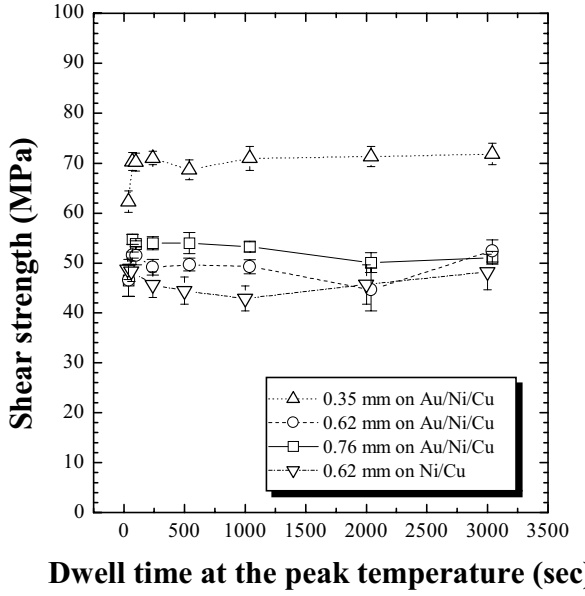

Fig. 2. Shear strength of the 63Sn-37Pb solder bumps as a function of the dwell time at 220 ℃.

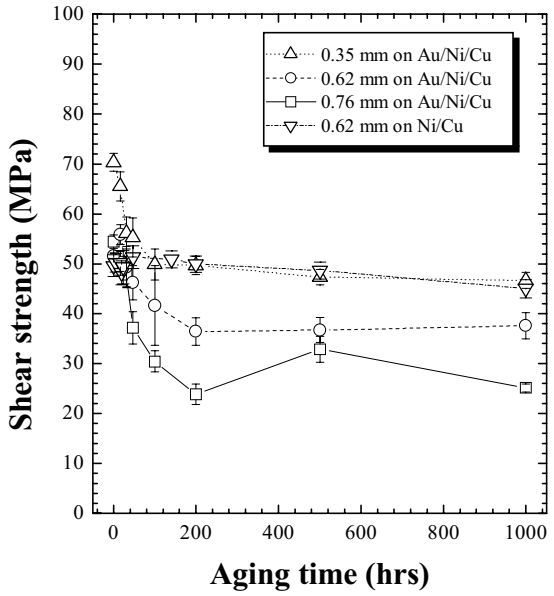

Fig. 3. Shear strength of the 63Sn-37Pb solder bumps with variation of aging time at 150°C.

Fig. 4 shows the fracture surface of the solder bumps after shear test. For the as-reflowed solder bumps, crack was initiated at the place of 0.04 mm above the solder ball pad, because the shear tip was located at 0.05 mm above the solder mask during shear test. The failure mode of the 63Sn-37Pb solder bumps, fabricated on Au/Ni/Cu UBM, was changed with the aging time.

At the early stage of aging, failure occurred within the solder bumps (ductile fracture). With increasing the aging time, however, the failed place was changed to the solder/intermetallic interfaces (brittle fracture) and finally to the Pb-rich layers. Contrary to the 63Sn-37Pb solder bumps formed on the Au/Ni/Cu UBM, solder bumps fabricated on the Ni UBM showed ductile fracture regardless of the aging time.

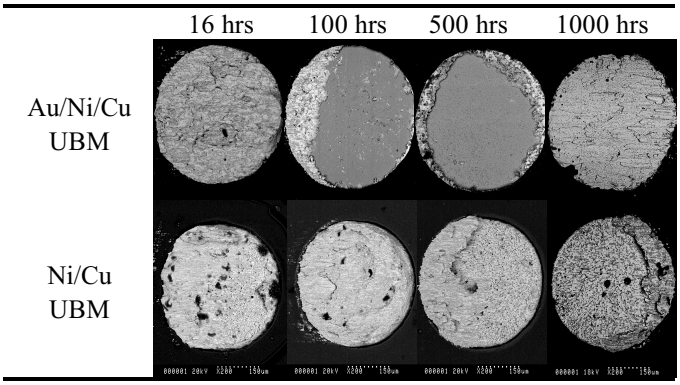

Fig. 4. SEM fractographs observed on the sheared surface of the 63Sn-37Pb solder bumps of 0.620 mm size which were aged for different times.

Figs.5 and 6 show thickness change of the $(Au,Ni)Sn_4$ and Ni_3Sn_4 intermetallic layers with the aging time. Growth rate of the $(Au,Ni)Sn_4$ intermetallic layer shows reverse relationship with the solder bump size. High growth rate on the solder bumps of 0.35 mm size seems to be attributed to the high Au concentration (Table 2). SEM observation revealed that thicker $(Au,Ni)Sn_4$ layer was formed at the edge of bump than at the center regardless of the bump size. As shown in Fig. 6, the growth rate of Ni_3Sn_4 intermetallic layer was almost same for the 63Sn-37Pb solder bumps formed on Au/Ni/Cu UBM without depending on the bump size. However, Ni_3Sn_4 intermetallic layer of the solder bumps formed on the Ni UBM grew substantially with increasing the aging time. Fig. 3 showed that the shear strength of the 63Sn-37Pb solder bumps on Ni/Cu UBM was not almost changed with aging, while the shear strength of the bumps on Au/Ni/Cu UBM decreased. From comparisons of the results in Figs. 3, 5, and 6, transition of the failure mode with aging could be attributed to the growth of $(Au,Ni)Sn_4$ rather than Ni_3Sn_4. As the thickness of the $(Au,Ni)Sn_4$ layer reached a critical value with aging treatment, lattice strain at the $(Au,Ni)Sn_4/Ni_3Sn_4$ interface, originated from the formation of $(Au,Ni)Sn_4$ [10], caused brittle farcture along the $(Au,Ni)Sn_4/Ni_3Sn_4$ interface.

Shear strength and aging characteristics of the Sn-Ag-Bi solder bumps

Fig. 7 shows the tensile strength of the Sn-Ag-Bi solder alloys, as-casted and aged at 150°C for 300 hours, as a function of the Bi content. Foth both as-casted and aged samples, the tensile strength increased with increasing the Bi content.

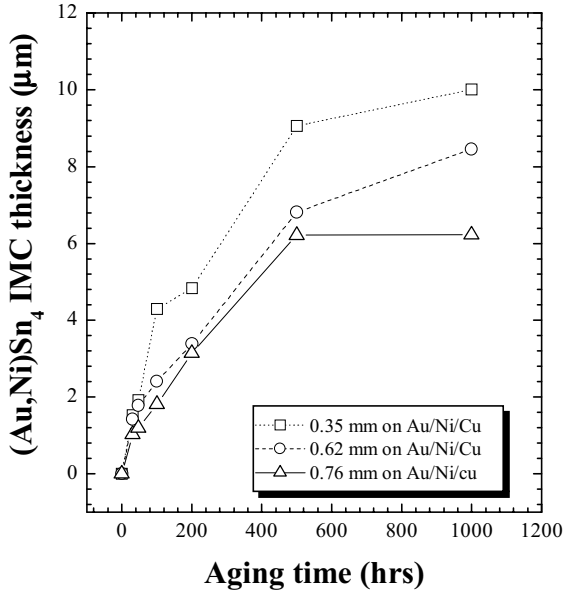

Fig. 5. $(Au,Ni)Sn_4$ thickness of the 63Sn-37Pb bumps as a function of the aging time at 150°C.

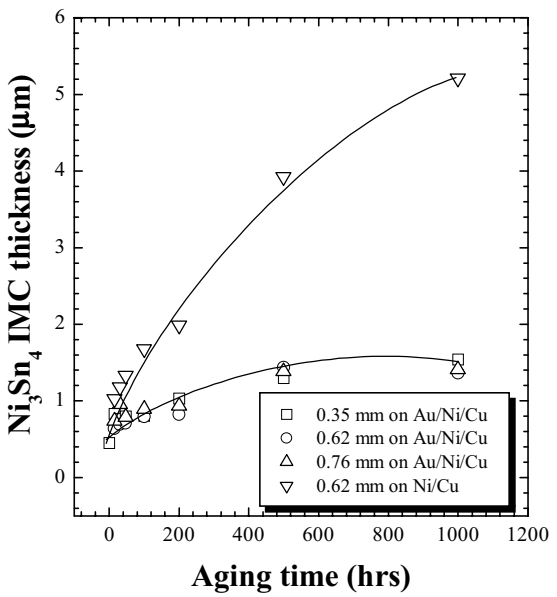

Fig. 6. Ni_3Sn_4 thickness of the 63Sn-37 bumps as a function of the aging time at 150°C.

While the increase of the tensile strength with addition of Bi up to 5 wt% could be due to solid solution hardening, addition of Bi over the solid solution limit would contribute to the strength increment through Bi precipitation [11,12]. The tensile strength of the Sn-Ag-Bi solder alloys was little changed with aging treatment for 300 hours.

The shear strength changes of the Sn-3.5Ag-Bi solder bumps, reflowed at 240°C for 30-180 seconds, are shown as a function of the Bi content in Fig. 8. Generally, the shear strength increased with increasing the Bi content and reached maximum at 5-7 wt% Bi. Shear strength of the Sn-3.5Ag-7Bi and Sn-3.5Ag-9Bi solder bumps decreased with increasing the dwell time from 120 seconds to 180 seconds due to the BT substrate fracture. Fig. 9 shows variation of the shear strength of the Sn-3.5Ag-Bi solder bumps formed on Au/Ni/Cu UBM with the aging time at 150°C. Shear strength of the Sn-3.5Ag-5Bi solder bumps increased substantially from 70 MPa to 84 Mpa with increasing the aging time to 300 hours. Fig. 10 and Fig. 11 show the fractographs observed on the sheared surface of the Sn-Ag-Bi bumps. In case of the as-reflowed solder bumps, as shown in Fig. 11, failure occurred within the solder bumps regardless of the Bi content. The Sn-3.5Ag and Sn-3.5Ag-1Bi solder bumps showed ductile fracture behavior even aged for 300 hours. However, failure mode of the Sn-3.5Ag-5Bi bumps was changed from ductile to brittle fracture with increasing the aging time. The fracture surface of the Sn-3.5Ag-5Bi was covered with the very thin solder alloy layer (Fig. 10). In general, such failure occurs when the interfacial strength is less than the flow stress of the solder bump. Similarly, fracture of the Sn-3.5Ag-9Bi solder occurred at the solder/intermetallic interface.

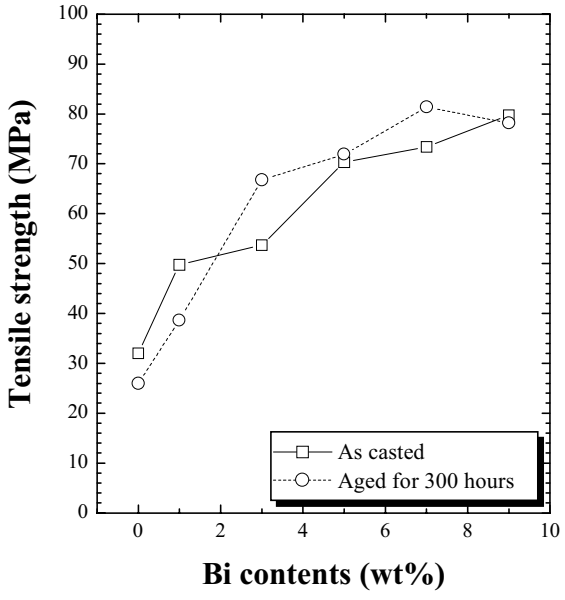

Fig. 7. Tensile strength of the Sn-3.5-Bi solder alloys as a function of the Bi content.

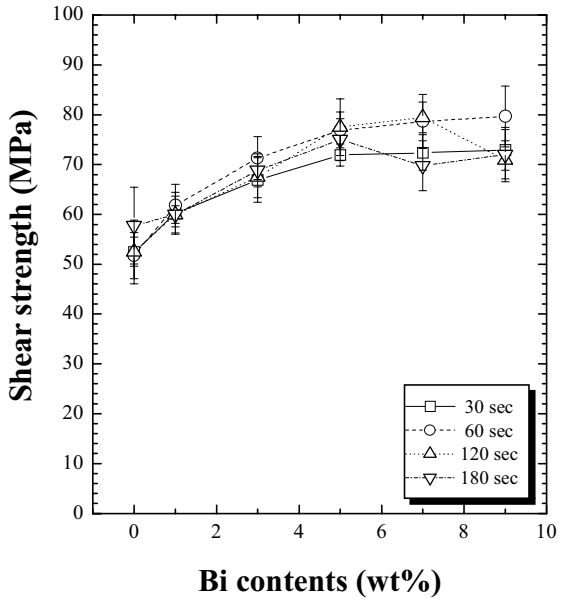

Fig. 8. Shear strength of the Sn-3.5Ag-Bi bumps, reflowed at 240°C for various time, as a function of the Bi content.

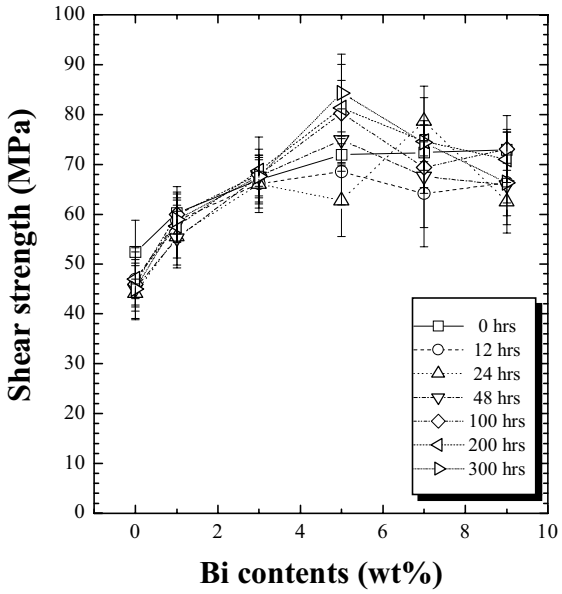

Fig. 9. Shear strength of the Sn-3.5Ag-Bi bumps, aged at 150°C for various time, as a function of the Bi content.

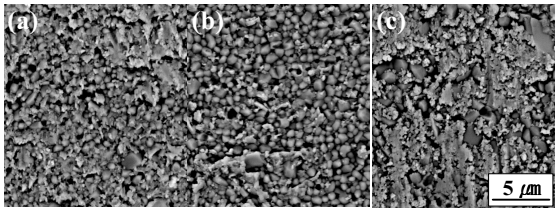

Fig. 10. SEM fractographs observed on the sheared surface of the Sn-3.5Ag-5Bi solder bumps aged at 150°C. (a) 48 hours, (b) 100 hours, and (c) 300 hours.

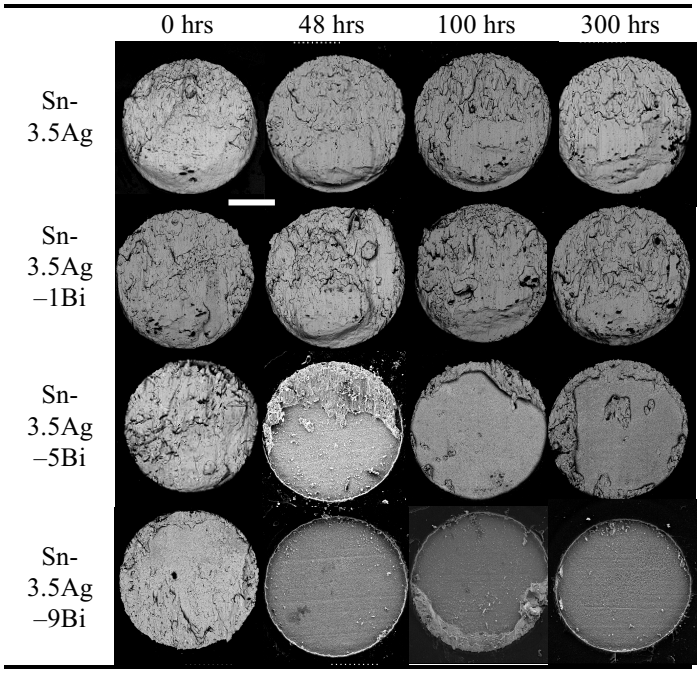

Fig. 10. SEM fractographs observed on the sheared surface of the Sn-3.5Ag-Bi solder bumps aged at 150°C.

Conclusions

(1) Ball shear strength of the 63Sn-37Pb solder bumps, formed on Au/Ni/Cu UBM, was dependent on the bump size. The shear strength of the solder bumps of 0.35 mm size was higher than those of the 0.62 and 0.76 mm size, which could be attributed to precipication hardening with Au-Sn intermetallic compounds. When the bump size was identical, the 63Sn-37Pb solder bumps exhibited higher shear strength on Au/Ni/Cu UBM than on Ni/Cu UBM.

(2) Although the shear strength of the 63Sn-37Pb solder bumps on Au/Ni/Cu UBM decreased with the aging treatment at 150°C, the shear strength of the 63Sn-37Pb solder bumps was kept almost constant on Ni/Cu UBM even after aging for 1000 hours.

(3) With increasing the aging time, the failure mode of the 63Sn-37Pb solder bumps, fabricated on the Au/Ni/Cu UBM, was changed from ductile fracture (solder failure) to brittle fracture (interface failure). Contrary to this, the 63Sn-37Pb solder bumps formed on Ni UBM showed ductile fracture regardless of the aging time up to 1000 hours.

(4) Tensile strength of the Sn-3.5Ag-Bi alloys increased with increasing the Bi content up to 9 wt% due to solid solution hardening and precipitation hardening.

(5) Ball shear strength of the Sn-3.5Ag-Bi solder bumps increased with increasing the Bi content and reached maximum at 5-7 wt% Bi. Shear strength of the Sn-3.5Ag-5Bi solder bumps increased substatially from 70 MPa to 84 MPa by aging at 150°C for 300 hours.

(6) The locus of failure was changed from solder interior to the solder/intermetallic interface as Bi content and aging time increased.

Acknowledgement

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Substrate Designs To Improve Die Crack Damage in CSP

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Abstract

For a growing development and design of high performance IC, more and more functions are demanded to contain in a Chip Scale Package (CSP) for the application that requires low profiles and small footprints. With thinner package profile requirement, thinner substrate is necessary. More reliability issues arise with thinner substrate to provide the mechanical support. Due to the different kinds of the design layout of the substrate, they induce different stress distribution to affect the IC chip directly during various assembly processes. These propagating effects may finally cause the die crack damage. Therefore, proper substrate layout design does not only achieve the thermally and electrically functional requirement, but also prevent critical mechanical problems.

The purpose in this paper is to investigate mechanical effects on the IC chip with different substrate design patterns. Further, to improve this influence by the optimal layout on the substrate, the dummy copper layer is used within the substrate. For comparison and confirmation of these phenomena, both numerical analysis (FEA) and experiment measurement were employed. CSPs were taken as the test vehicle. Effect of dummy patterns was observed during the assembly process. There is no chip damage observed with modified substrate design. Further investigating other possible factors, substrate thickness was varied in FEA model. It was proved that the design effect is insignificant with thicker substrate thickness. Similar result was observed with parameters of chip thickness, and Moiré interferometry was engaged to verify FEA models.

Introduction

Definition of Chip Scale Packages (CSP) is that a whole bare die is occupied 80% and above of the package, so the profile can be as small as possible. Better electrical performance can be expected with shorter interconnection. It can be used in memory, micro-processors/controllers, Flash, SRAM, DRAM, ASICs, DSPs and RF devices.

A Thin and Fine-pitch BGAs (TFBGA) was taken as the test vehicle. Fig. 1 shows the typical TFBGA structure. TFBGAs are cavity up, wire bonded, and overmolded on rigid substrate chip scale packages. They offer small scale and light weight as well as cost saving solution for low ball counts less than 300. TFBGA with a matrix format substrate and a common mold chase accommodates different package sizes to offer manufacturing flexibility and thus reduce time to market effectively. But the thin substrate and mold body will cause structure problems during manufacturing, ex. warpage, die crack and wire exposure.

Recently, the numerical analysis is used extensively to estimate stress and strain in package structure, but in general the numerical model gives the results uncertainly due to complexity of the package structure and the material properties. Therefore, the experiment verification of the numerical model becomes more important for the product design. The verification and prediction of the numerical model become an integral part of electronic packaging product development in order to reduced cost and cycle time. In this paper, the moiré interferometry with phase shifting method was employed to study the in-plane displacements under thermal loading conditions.

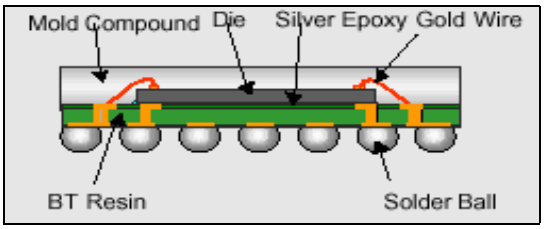


Fig. 1 Typical TFBGA structure

Die crack damage

A die crack phenomenum was found out during the development stage. Fig. 2 shows the die crack patterns and the phenomenum observed by SAT and decap analysis. A square shape of crack line are on the surface of die. It is find out after molding process, no die crack after the die bonding and wire bonding process. But after molding process, the die crack happened again after molding transfer pressure raising. Therefore, it must be confirmed within the molding process.

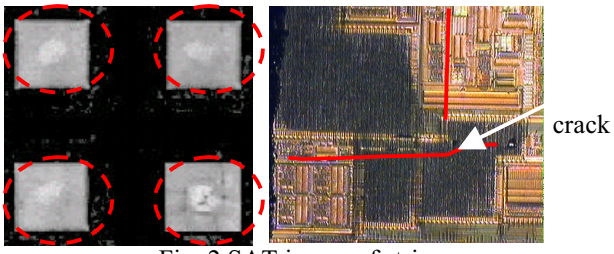


Fig. 2 SAT image of strip.

Substrate layout

Since the power dissipation of the device is not high, there is no thermal ball required under the die. Therefore, these is no Cu trace designed under the die. This makes a thinner region under the die. The thickness of copper layer is about 20μm, and Fig. 3 shows a gap between the bottom of the substrate and mold tool.

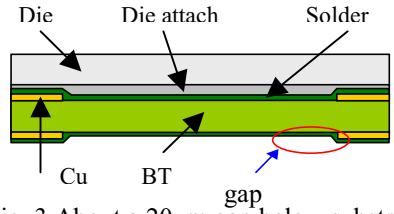


Fig. 3 About a 20μm gap below substrate.

Therefore, if there is no enough fully support on the bottom of chip, the bending stress and shear stress will cause the die crack after molding. The crack on the center of the chip was caused by external force from die top since the middle is lower than outer area. Because the chip is a brittle material and can not bear the stress when the molding pressure raising. Fig. 4 shows a crack mechanism by external force. From the crack pattern, the crack position and shape are matched with the substrate pattern. The location of die crack is right at the edge of Cu and BT. It is suspected that ununifom Cu layer is the root cause of the cracking phenomenon.

The die crack is also find out after modifying the parameter of die bonding and wire bonding. Therefore, the needle speed of die bonding and the wire bonding force were not cause of the die crack. It is necessary to redesign the substrate. So, to add the dummy copper layer in the middle area of both top and bottom layers of substrate is one of the methods to reduce the stress in this case.

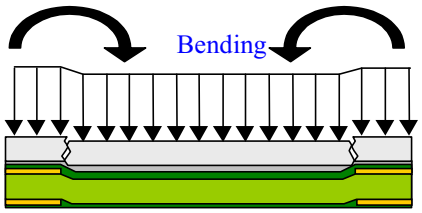


Fig.4 A crack mechanism by external force.

In fact, the different kinds of the design layout will cause different die crack phenomenum. Fig. 5 shows another die crack patterns. This package has a high ratio of the length versus width (2.33 times), and the crack on the both sides of the die was also caused by external force. In this case, the dummy copper layer in the sides of the substrate are added.

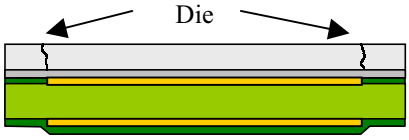


Fig. 5 Another die crack patterns.

The purpose in this paper is to investigate mechanical effects on the IC chip with different substrate design patterns. [1,2] Further investigating other possible factors, substrate thickness was varied in FEA model. It was verified that dummy pattern does help to reduce the stress on chip. However, it was proved that the design effect is insignificant with thicker substrate. Similar result was observed with parameters of chip thickness, and Moiré Interferometry was engaged to verify FEA models.

Numerical analysis

FEM simulation model

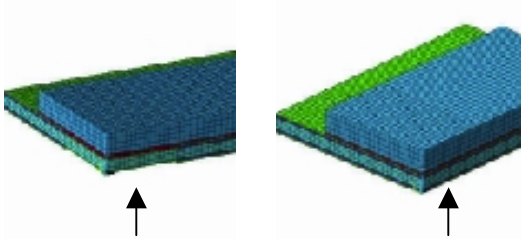
In this paper, three dimension finite element models are employed to investigate the thermal mechanical induced stress. The purpose is to compare the stress effects for different locations of copper pattern in the substrate and adding a dummy pattern for further research.

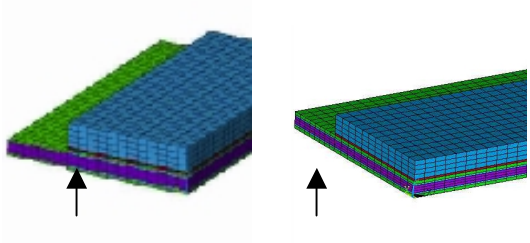
ANSYS V5.6 was used and assumes that (a). all materials are homogeneous, isotropic, linear elastic; (b). Material interfaces within the package have perfect adhesion; (c). Young's modulus and coefficient of thermal expansion are temperature independent; (d). applied a symmetric molding pressure on the chip surface. (e). only one quarter of the package is modeled.

Material properties of TFBGA are shown in Table 1. The different thicker substrate and chip thickness will be simulated in this paper. Two kinds of the the design layout also will be simulated. Type I is adding a dumy pattern in the center area, and Type II is adding a dummy pattern in both sides. Fig. 6 and 7 shows the one-Forth finite element model with and without dummy pattern of Type I and Type II.

Item \ Properties		Young's modulus (kg/mm^2)	CTE (ppm/ ^{o}C)	Tg(^{o}C)
Chip		16000	2.7	~
Die-attach		127	80/154	27
M/C		1500	13/45	200
Substrate	BT	2451/980	14/58	190
	Copper	12,100	16.3	~

Table 1: Material properties of TFBGA package.


(a). w/o dummy pattern, (b). w/ dummy pattern
Fig. 6 Type I: One-Forth finite element model shows the chip


(a). w/o dummy pattern, (b). w/ dummy pattern
Fig. 7 Type II: One-Forth finite element model shows the chip

Simulation result

Stress effect of thermal loading and molding pressure

Table 2 shows the stress in the chip bottom after thermal loading condition and pressure loading condition of Type I. All chip thickness are the same (12mils). The thermal loading

and pressure loading condition was simulating the cooling process after molding and the pressure loading under molding, respectively.

In this case, the thermal loading is from 175• to 25• and the pressure loading was assumed 4.6kg/mm^2. The result shows that the pressure loading under molding was the root cause that leads to the die crack. Because of the stress in the chip bottom had a large difference between without and with dummy layer, but it's no difference in thermal loading condition.

Loading condition	w/o dummy layer	w/ dummy layer	Reduction (%)
Thermal	58.09	58.00	0.15
Pressure	55.94	6.26	87.98

Unit: kg/mm^2

Table 2: The stress with different loading condition.

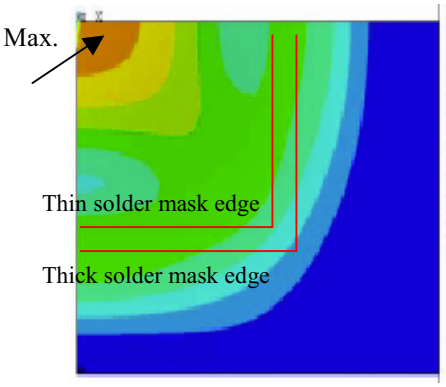
Dummy pattern effect

The substrates without dummy layer will cause much large stress effect in the chip bottom. The thinner thickness of the substrate, it will get much worst effect. If the package without a fully copper traces spreading in the substrate, the solder mask covering form a thickness drop under die. This structure induced large stress effects on the die because the supporting strength is too weak. Moreover, the substrates have better performance with a dummy layer and reduced to 1/10 stress on the chip bottom for both Type I and Type II. Therefore, to add a dummy layer is effective in reducing stress. Fig. 8 and 9 are show the stress distribution in chip bottom of Type I and Type II. It has a maximum compression stress of solder mask profile changes. The different thickness of the solder mask region is highlighted by red line.

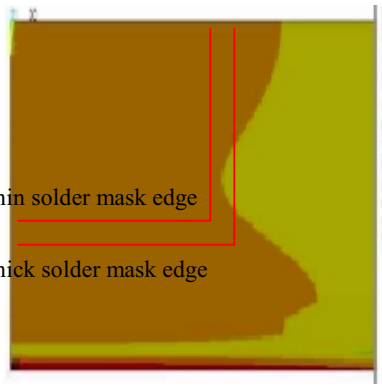
Substrate pattern	w/o dummy layer	w/ dummy layer	%
Type I	55.94	6.26	11.19
Type II	52.91	5.18	9.79

Unit: kg/mm^2

Table 3: Different substrate pattern simulation result.

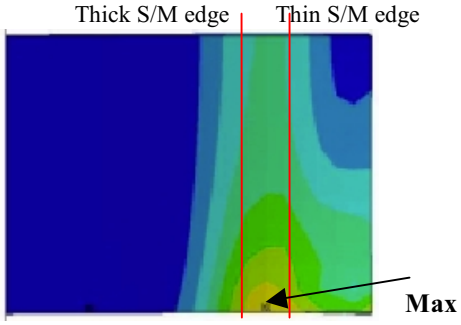


(a). Stress distribution without dummy layer.

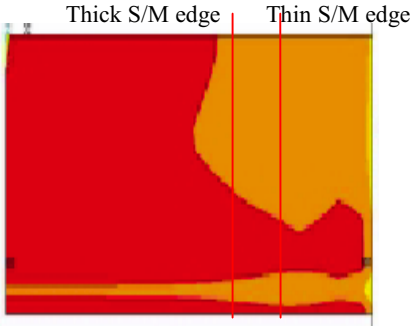


(b). Stress distribution with dummy layer.

Fig. 8 Chip bottom stress distribution of Type I.



(a). Stress distribution without dummy layer.



(b). Stress distribution with dummy layer.

Fig. 9 Chip bottom stress distribution of Type II.

Substrate thickness effect

Fig. 10 shows the chip bottom stress with different substrate thickness. It can be seem that the thinner substrate (0.21mm) without dummy layer have a large stress than other thickness (0.36 and 0.56 mm), and a substrate with dummy layer can reduce more stress.

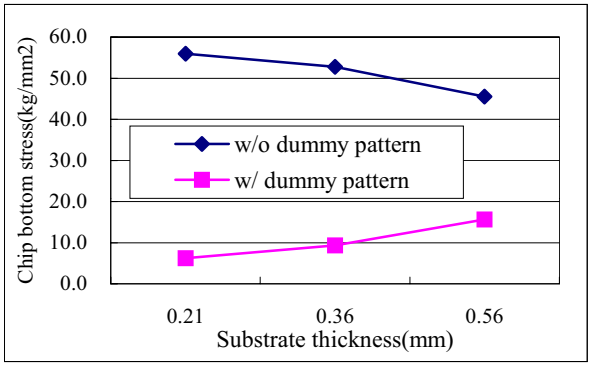


Fig. 10 Chip bottom stress with different substrate thickness.

Chip thickness effect

The result is shown in Fig.11 for different chip thickness. The stress variation was slight. Increasing the chip thickness does not enhance the chip strength under molding pressure as original expected.

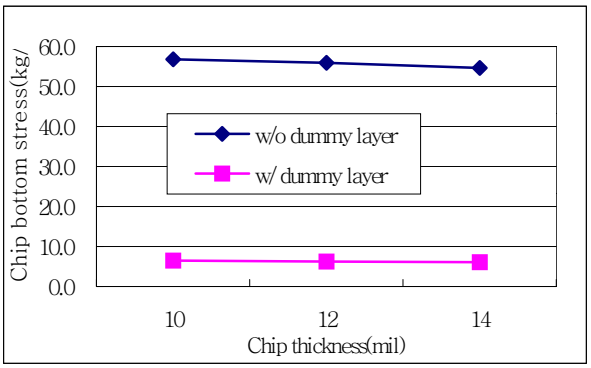


Fig. 11 Chip bottom stress with different chip thickness.

Experimental analysis

Moiré Interferometry with phase shifting method

Moiré Interferometry is an optical technique which providing whole-field contour maps of in-plane displacement field U and V on flat surfaces. It is not only used to verify FEM but also to observe insignificant difference of various design which might be neglected by FEM. A high frequency cross-line diffraction grating is replicated onto the cross-section and it deforms together with the underlying specimen at an elevated temperature.

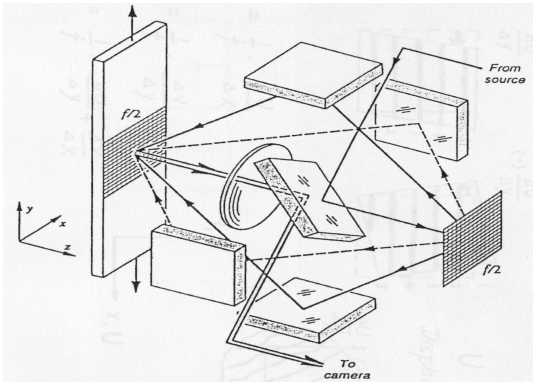


Fig. 12 Schematic diagram of moiré interferometry.

The sensitivity of the fringe analysis is increased by phase shifting technique and by precisely altering the phase angle. The reference grating is attached on a phase shift stage and controlled by a piezoelectric transducer (PZT) driver. The PZT stack controls the reference grating movement when certain voltage is applied to it. Based on a grating frequency of 1200 lines/mm, the each interference fringe spacing represents 417nm of specimen displacement. [3,4] If the reference grating is moved by 1/4 of the grating pitch along the grating direction, the fringes will be moved 1/4 fringe order. Since the spacing of one fringe is equal to a 2π phase angle, the moiré interference patterns after four precisely phase-shifted achieves the demand for phase shifting. Equation (1) describes the four images.

$$
\begin{aligned}
I_1(x,y) &= I_0(x,y) + I'(x,y)\sin[\varphi(x,y)] \\
I_2(x,y) &= I_0(x,y) + I'(x,y)\sin[\varphi(x,y) + \pi/2] \\
I_3(x,y) &= I_0(x,y) + I'(x,y)\sin[\varphi(x,y) + \pi] \\
I_4(x,y) &= I_0(x,y) + I'(x,y)\sin[\varphi(x,y) + 3\pi/2]
\end{aligned}
\qquad (1)
$$

where $I_0(x,y)$ is the background, and $I'(x,y)$ is the periodically varying intensities and $\varphi(x,y)$ is the phase term. Each subsequent pattern is shifted by a phase difference of exactly π/2 or 1/4 of the fringe period. The phase term $\varphi(x,y)$ is then solved as,

$$
\varphi(x,y) = \arctan\left[\frac{I_1(x,y) - I_3(x,y)}{I_2(x,y) - I_4(x,y)}\right] \qquad (2)
$$

Experimental procedure

Moiré interferometry has been an implemented to determine the thermal deformation of various electronic packaging products. [5,6] A diffraction grating with 1200lines/mm cross-line was replicated to the specimen after sectioning and polishing the package. The grating was applied to the cross-section at 100• using Tra-Bond F253 epoxy and was performed at room temperature, simulating a thermal load of -75•.

Measurement result

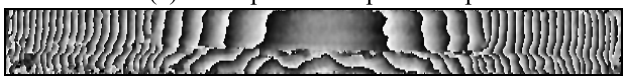
Moiré phase maps from phase shifting are shown in Fig. 13 and 14. The resulting fringe patterns represent contours of constant U and V displacement fields, defined as in-plane displacements in orthogonal X and Y directions, respectively. The U and V field moiré patterns with a contour interval of 0.417nm/fringe. In this measurement, the Type I substrate was be investigated.

(a). U-displacement phase map

(b). V-displacement phase map

Fig. 13 The displacement with dummy layer.

(a). U-displacement phase map



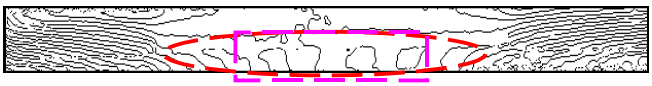
(b). V-displacement phase map

Fig. 14 The displacement without dummy layer.

In this result, the fringe pattern is a symmetric distribution in left side and right side. Both in die area and other areas have different distributions in U and V field. The fringe pattern in U field should be a vertical and uniform distribution in a linear or pure material. But in a composite material, it will depend on the material parameters. The slant fringe means that the package has shear deformations because it's a composite material.

The material properties had a slightly difference if add dummy pattern in theory, ex. CTE and Young's Modulus. Since only applied thermal loading in this case, so the influence of CTE can be observed. The fringe pattern number is a tight distribution in material interface of compound and chip. The deformation of substrate below the die is more uniform than below molding compound. And the CTE is a major cause to induce shear deformations.

Fig. 15 shows the displacement contour maps, and creates contour maps with 208.5nm resolution. In this result, the substrate with dummy layer had more u-displacements under the die (ellipse location), especial in dual side dummy layer area (rectangular location). The displacement of substrate under die area in U field is 1.668μm (8 orders fringes) and 8.340μm (4 orders fringes), respectively in Fig. 15a and 15b. But in the V field was similar under die. It is shown in Fig. 16. Therefore, if the difference with dummy layer was cause by mechanical loading, it's difficult to observe by thermal loading.



(a). with dummy layer.

(b). without dummy layer.

Fig. 15 U-displacement divide phase diagram.

(a). with dummy layer.

(b). without dummy layer.

Fig. 16 V-displacement divide phase diagram.

Verification

According to above simulation and experimental, both Type I and Type II are redesign the substrate pattern. They are shown in Fig17 and 18. Type I is to add a dummy layer in the middle area, and Type II is to add a dummy layer in both sides. The substrate after re-design has no die crack after molding process and O/S test. It also has a reliability testing under 30 • /70%RH/168hrs by three times, and TCT 1000cycles(-65•~150•), TST500cycles and PCT168hrs.

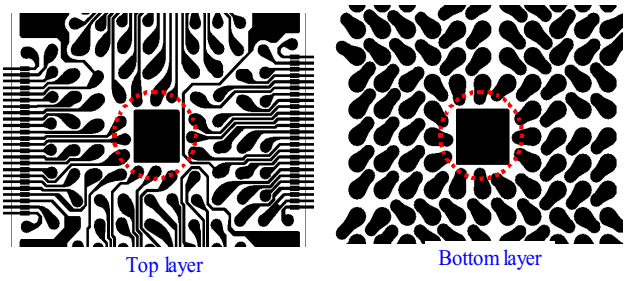


Fig. 17 Adding dummy layer in the middle area.

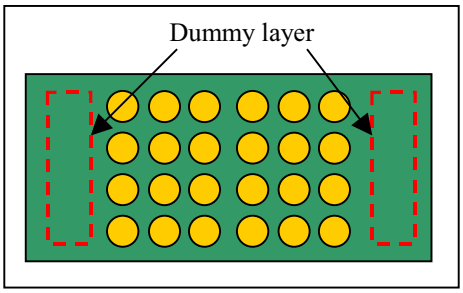


Fig. 18 Adding a dummy layers in both sides.

Conclusions

The simulation and experiment were carried out to study the die crack behavior with different substrate. In simulation result, the pressure loading under molding was the root cause that leads to the die crack. The structure induced large stress effects on the die because the supporting strength is too weak. It has a maximum compression stress with solder mask profile change. The substrate had a better performance with a dummy layer and reduced to 1/10 stress in the chip bottom. In experiment results, the substrate with dummy layer had more u displacement under die, especial in dual side metal layer area. So, to add a dummy layer is to provide a solution to reduce the die crack damage and to achieve the optimal structure.

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